REMARKS

The Examiner rejected claims 1 and 8 under 35 U.S.C. §102(e) as being unpatentable over Archibald Jr. et al. (US 2002/0184580).

The Examiner rejected claims 1, 9 and 26 under 35 U.S.C. §102(b) as being unpatentable over Adams et al. (US 5,912,901).

The Examiner has stated that claims 10-25 are allowable and claims 2-7 AND 27-33 would be allowable. Applicants gratefully acknowledge the Examiner's indication of allowable subject matter.

Applicants respectfully traverse the §102(b) and §102(e) rejections with the following arguments.

35 USC § 102

As to claim 1, the Examiner states that "Archibald et al. teaches " A method, computer readable medium, apparatus and RAID controller for performing nondestructive write testing is disclosed. Abstract first sentence. For data storage devices divided into sectors. Abstract second sentence. However, it will be appreciated that the media surface scanner 109 may be controlled so as to scan only selected portions of the media, to skip particular portions of the media, to scan selected portions of the media more or less frequently than other portions, or directed to scan according to other predetermined or programmatically constrained rules. [0023]. Desirably, the media surface scanner 109 will traverse all sectors on the media so that any media defect wherever located can be identified. [0023]. In other words, in response to an acceptable testing result, a sector is designated as "not identified. If no errors are detected during the read

phase of the test (step 306), the controller 100 will write back the read data to the sector (step 304). [0026]."

Applicants contend that claim 1, as amended, is not anticipated by Archibald Jr. et al. because Archibald Jr. et al does not teach each and every feature of claim 1. For example, Archibald Jr. et al. does not teach "said data comprising test data resultant from additional testing of said semiconductor device and unrelated to testing said selected portion of said memory.." Applicants respectfully point out that Archibald Jr. et al. teaches that test data stored in the memory is the data used to test the memory itself. Archibald Jr. et al. does not teach using the tested good memory for storing test data unrelated to the testing of memory. Further, Archibald Jr. et al. teaches testing spinning media such as hard drives, floppy drives and optical drives and not testing of semiconductor devices.

Based on the preceding arguments, Applicants respectfully maintain that claim 1 is not unpatentable over Archibald Jr. et al and is in condition for allowance. Since claims 2-9 depend from claim 1, Applicants respectfully maintain that claims 2-9 are likewise in condition for allowance.

As to claim 1, the Examiner states that Adams et al. teaches " With reference now to FIG. 1, there is illustrated a conventional closed-loop testing apparatus for an integrated circuit memory. Column 1, lines 35-37. As will be understood by those skilled in the art, memory array 32 comprises a number of individual memory cells which are each accessed for reading or writing data by selecting particular word and bit lines. Column 3, lines 6-9. Therefore, the selected portion of said memory is an individual memory cell. BIST 12 applies internally generated test data and address data to memory array 18 and compares output data read out from memory array 18 with expected data. Column 1, lines 45-48. In response to a discrepancy

between the output data and the expected data, BIST 12 indicates that failure within memory array 18 has been detected by driving diagnostic output (DGO) signal 20 high. Column 1, lines 48-51. Therefore, if there is an acceptable testing result, designated memory would be indicated by diagnostic output (DGO) signal 20 low. If a memory is determined to be error free, it is notoriously well known to those skilled in the art at the time of applicants' invention to se said memory for data storage and this is implied in the disclosure of Adams et al. since his invention is assumed by the patenting process to be useful."

Applicants contend that claim 1, as amended, is not anticipated by Adams et al. because Adams et al. does not teach each and every feature of claim 1. For example, Adams et al. does not teach "said data comprising test data resultant from additional testing of said semiconductor device and unrelated to testing said selected portion of said memory." Applicants respectfully point out that Adams et al. teaches that test data stored in the memory is the data used to test the memory itself. Adams et al. does not teach using the tested good memory for storing test data unrelated to the testing of memory.

Based on the preceding arguments, Applicants respectfully maintain that claim 1 is not unpatentable over Adams et al. and is in condition for allowance. Since claims 2-9 depend from claim 1, Applicants respectfully maintain that claims 2-9 are likewise in condition for allowance.

As to claim 26, the Examiners states that Adams et al teaches: " With reference now to FIG. 1, there is illustrated a conventional closed-loop testing apparatus for an integrated circuit memory. Column 1, lines 35-37. Or array built-in self test (ABIST) and will hereinafter be referred to generically as BIST. BIST 12 applies internally generated test data and address data to memory array 18 and compares output data read out from memory array 18 with expected data. Column 1, lines 45-40."

Applicants contend that claim 26 is not anticipated by Adams et al because Adams et al does not teach each and every feature of claim 26. For example, Adams et al does not teach "said test data comprising data unrelated to testing said memory" Applicants respectfully point out that Adams et al. teaches that test data stored in the memory is the data used to test the memory itself. Adams et al. does not teach using the tested good memory for storing test data unrelated to the testing of memory.

Based on the preceding arguments, Applicants respectfully maintain that claim 26 is not unpatentable over Adams et al and is in condition for allowance. Since claims 27-33 depend from claim 26, Applicants respectfully maintain that claims 27-33 are likewise in condition for allowance.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that claims 1-33 meet the acceptance criteria for allowance and therefore request favorable action. If Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invite the Examiner to contact the Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0456.

Respectfully submitted,
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